

Designer's™ Data Sheet

NPN Silicon Power Transistors**1 kV SWITCHMODE Series**

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

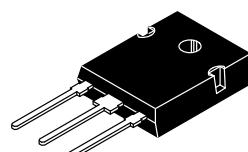
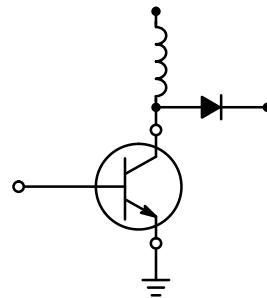
Features:

- Collector-Emitter Voltage — $V_{CEO} = 1000$ Vdc
- Fast Turn-Off Times
50 ns Inductive Fall Time — 100°C (Typ)
90 ns Inductive Crossover Time — 100°C (Typ)
900 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
Reverse-Biased SOA with Inductive Load
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability

MJW16010A*

*Motorola Preferred Device

POWER TRANSISTORS
15 AMPERES
500 VOLTS
125 AND 175 WATTS



CASE 340F-03
TO-247AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	500	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	Vdc
Emitter-Base Voltage	V_{EB}	6	Vdc
Collector Current— Continuous — Peak(1)	I_C I_{CM}	15 20	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$ Derate above $T_C = 25^\circ\text{C}$	P_D	135 54 1.09	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	I_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.92	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

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REV 3

MJW16010A
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	500	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	0.003 0.020	0.15 1.0	mA
Collector Cutoff Current (V _{CE} = 1000 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	0.020	1.0	mA
Emitter Cutoff Current (V _{EB} = 6 Vdc, I _C = 0)	I _{EBO}	—	0.005	0.15	mA

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 14a or 14b
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 1 Adc) (I _C = 10 Adc, I _B = 2 Adc) (I _C = 10 Adc, I _B = 2 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	0.25 0.45 0.60	0.7 1 1.5	Vdc
Base-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 2 Adc) (I _C = 10 Adc, I _B = 2 Adc, T _C = 100°C)	V _{BE(sat)}	— —	1.2 1.2	1.5 1.5	Vdc
DC Current Gain (I _C = 15 Adc, V _{CE} = 5 Vdc)	h _{FE}	5	8	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 kHz)	C _{ob}	—	—	400	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)						
Storage Time	(I _C = 10 Adc, I _{B1} = 1.3 Adc, V _{BE(off)} = 5 Vdc, V _{CE(pk)} = 400 Vdc)	(T _J = 100°C)	t _{sv}	—	900	2000
Fall Time			t _{fi}	—	50	250
Crossover Time			t _c	—	90	300
Storage Time		(T _J = 150°C)	t _{sv}	—	1100	—
Fall Time			t _{fi}	—	70	—
Crossover Time			t _c	—	120	—
Resistive Load (Table 2)						
Delay Time	(I _C = 10 Adc, V _{CC} = 250 Vdc, I _{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I _{B2} = 2.6 Adc, R _{B2} = 1.6 Ω)	t _d	—	25	100
Rise Time			t _r	—	325	600
Storage Time			t _s	—	1300	3000
Fall Time			t _f	—	175	400
Storage Time		(V _{BE(off)} = 5 Vdc)	t _s	—	700	—
Fall Time			t _f	—	80	—

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

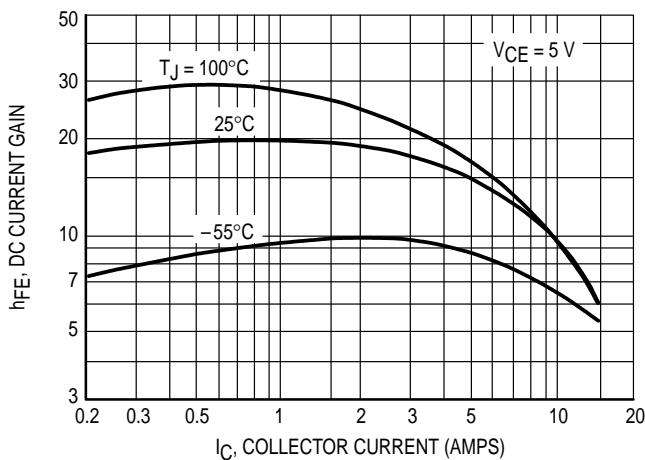


Figure 1. DC Current Gain

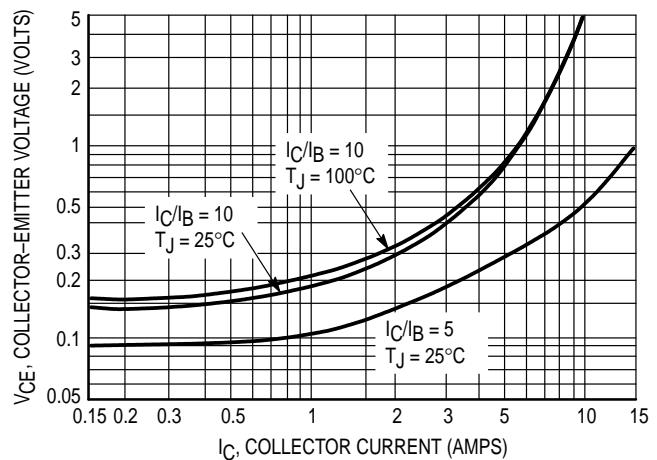


Figure 2. Collector-Emitter Saturation Region

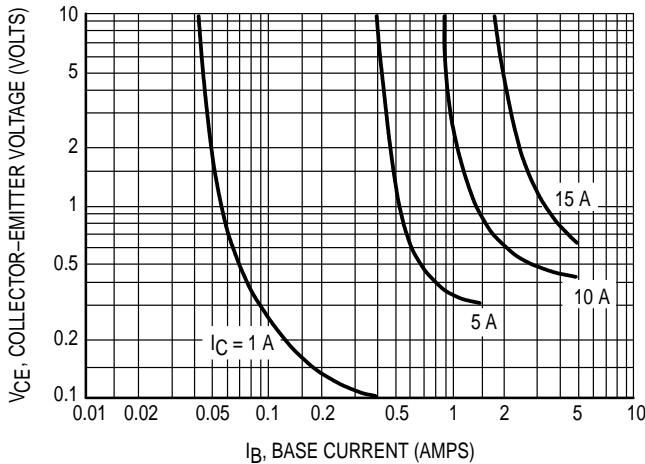


Figure 3. Collector-Emitter Saturation Region

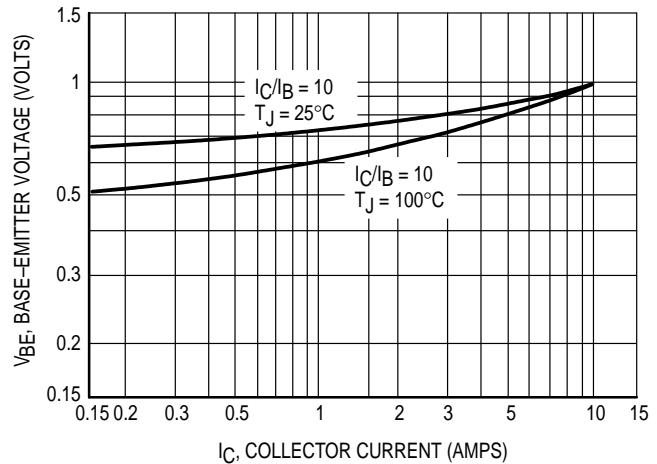


Figure 4. Base-Emitter Saturation Region

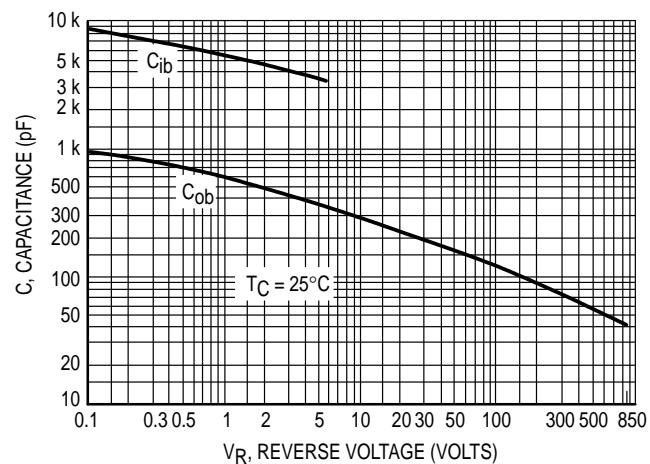


Figure 5. Capacitance

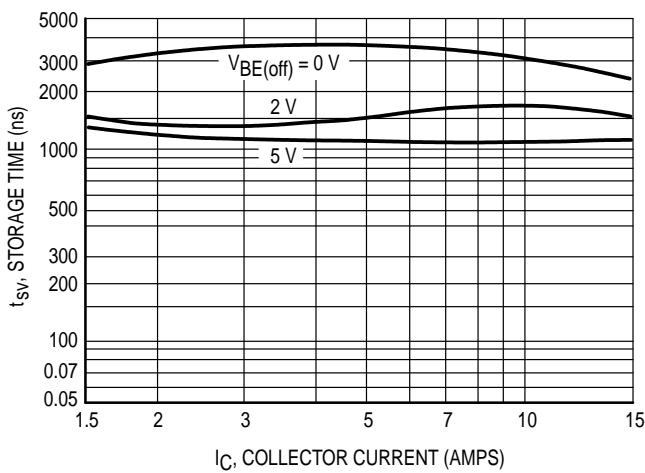
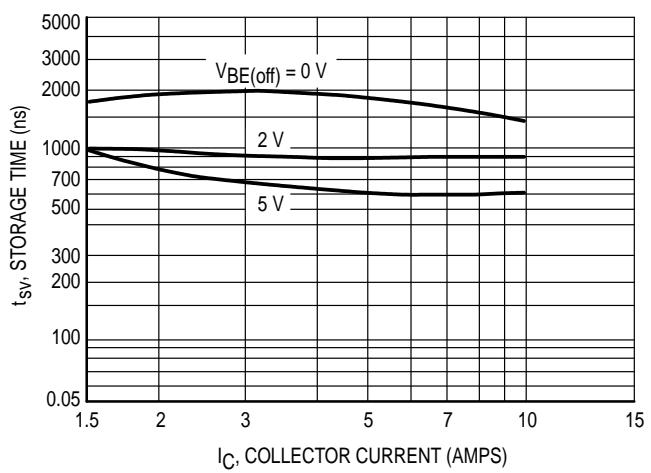
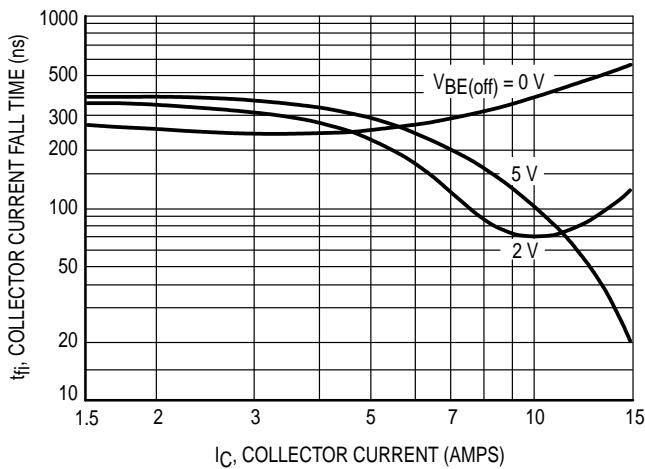
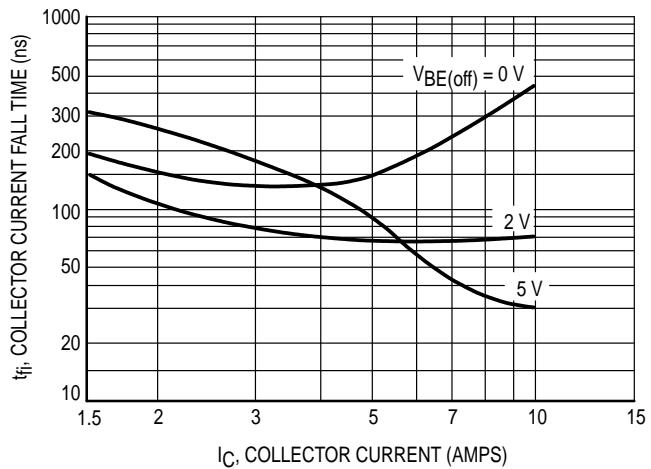
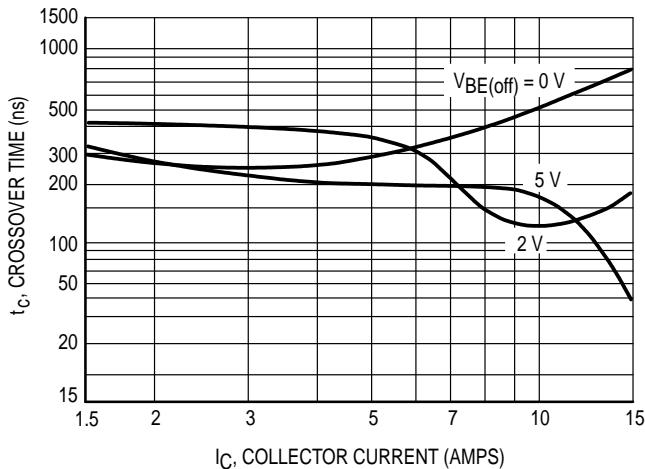
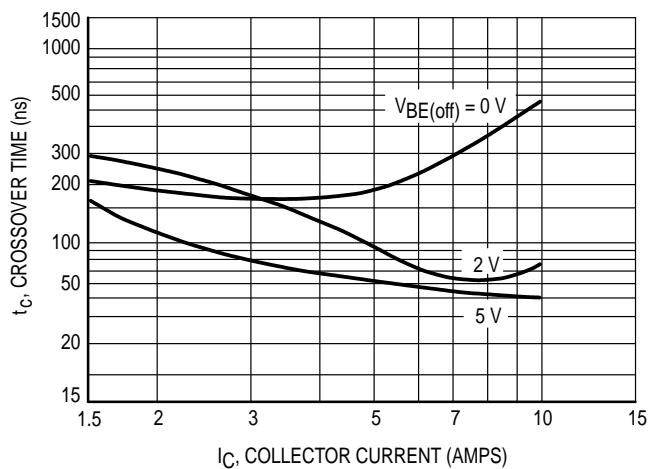
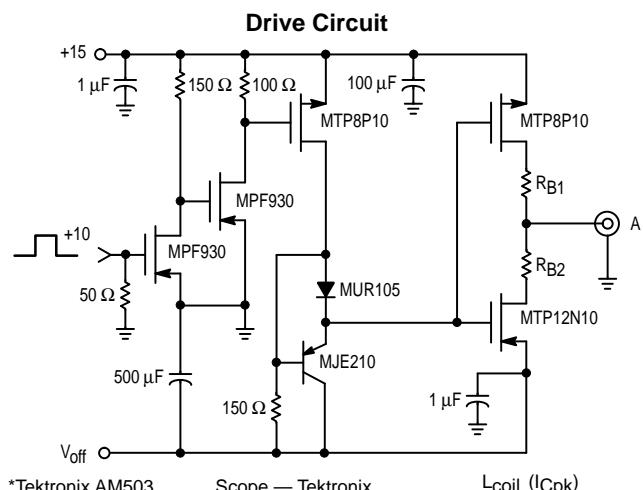
TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS $I_C/I_{B1} = 5, T_C = 75^\circ\text{C}, V_{CE}(\text{pk}) = 400 \text{ V}$ **Figure 6. Storage Time** $I_C/I_{B1} = 10, T_C = 75^\circ\text{C}, V_{CE}(\text{pk}) = 400 \text{ V}$ **Figure 7. Storage Time****Figure 8. Collector Current Fall Time****Figure 9. Collector Current Fall Time****Figure 10. Crossover Time****Figure 11. Crossover Time**

Table 1. Inductive Load Switching

*Tektronix AM503
P6302 or EquivalentScope — Tektronix
7403 or Equivalent

$$T_1 \approx \frac{L_{coil} (I_{C(pk)})}{V_{CC}}$$

$$T_1 \text{ adjusted to obtain } I_{C(pk)}$$

Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CEO(sus)}$
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$
 $I_{C(pk)} = 100 \text{ mA}$

Inductive Switching

$L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

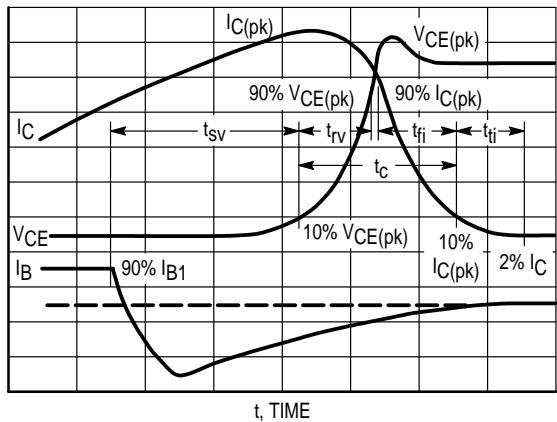
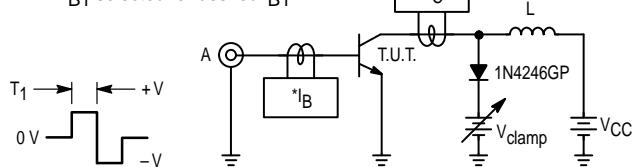


Figure 12. Inductive Switching Measurements

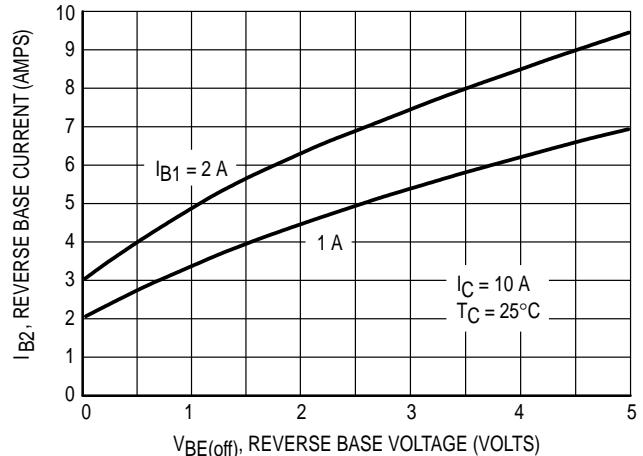
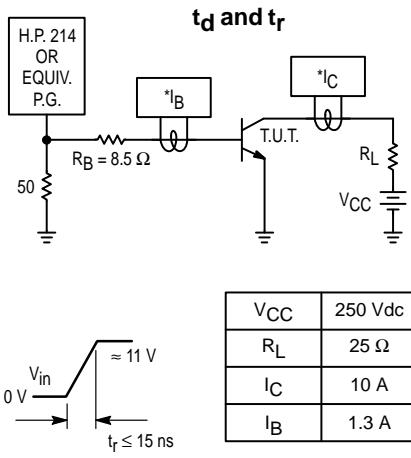
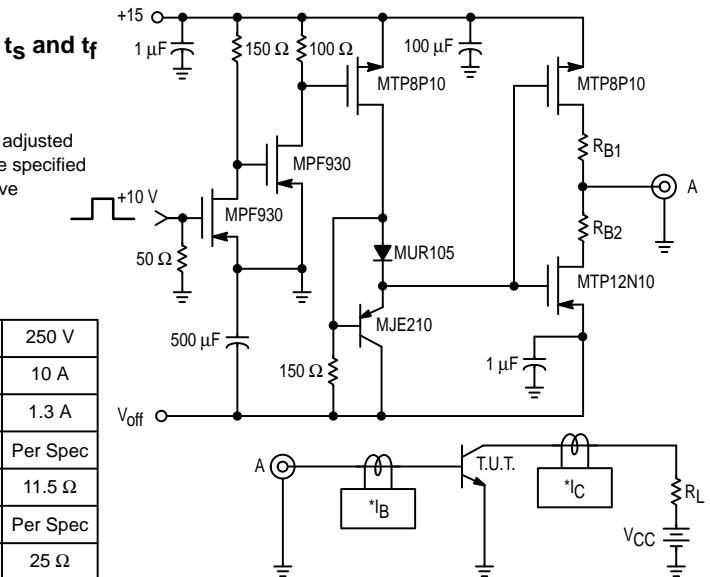


Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching

*Tektronix AM503
P6302 or Equivalent

V _{CC}	250 Vdc
I _C	10 A
I _{B1}	1.3 A
I _{B2}	Per Spec
R _{B1}	11.5 Ω
R _{B2}	Per Spec
R _L	25 Ω



GUARANTEED OPERATING AREA INFORMATION

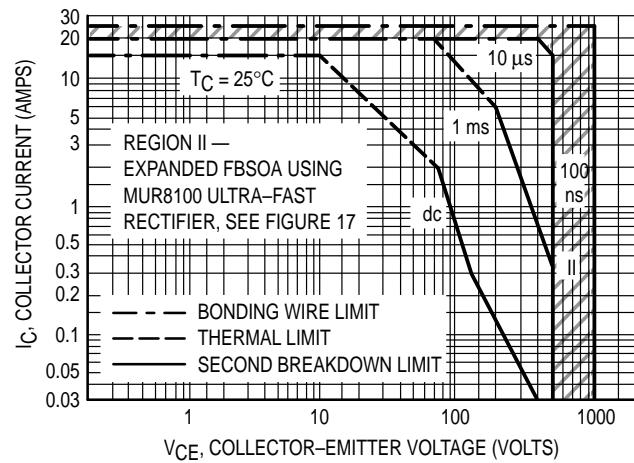


Figure 14. Maximum Rated Forward Biased Safe Operating Area

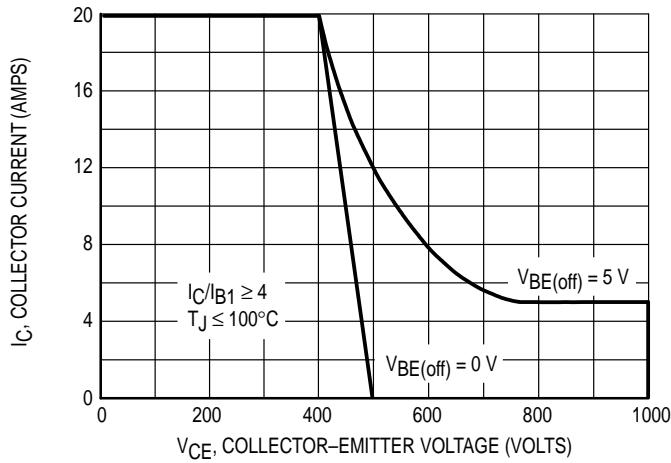


Figure 15. Maximum Reverse Biased Safe Operating Area

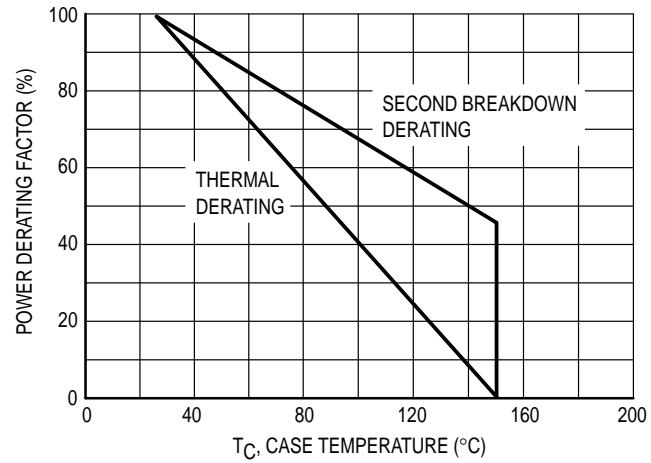


Figure 16. Power Derating

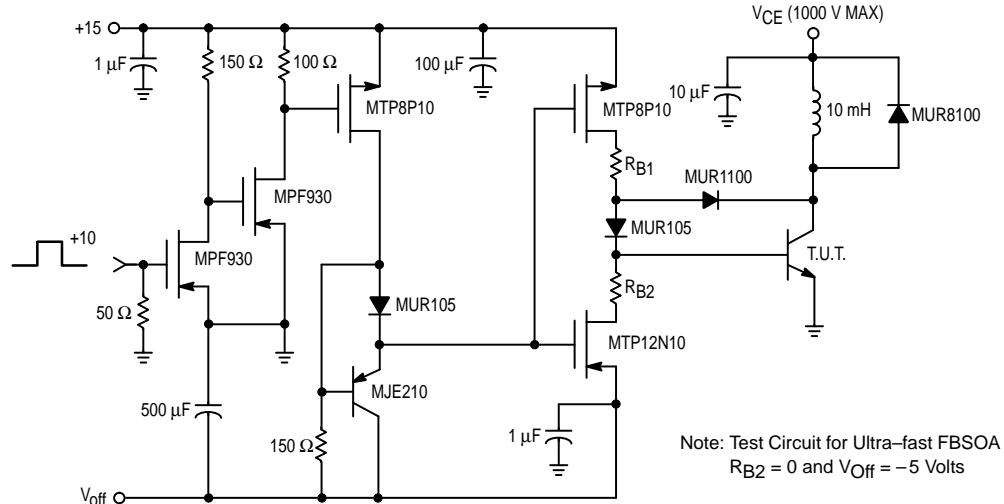


Figure 17. Switching Safe Operating Area

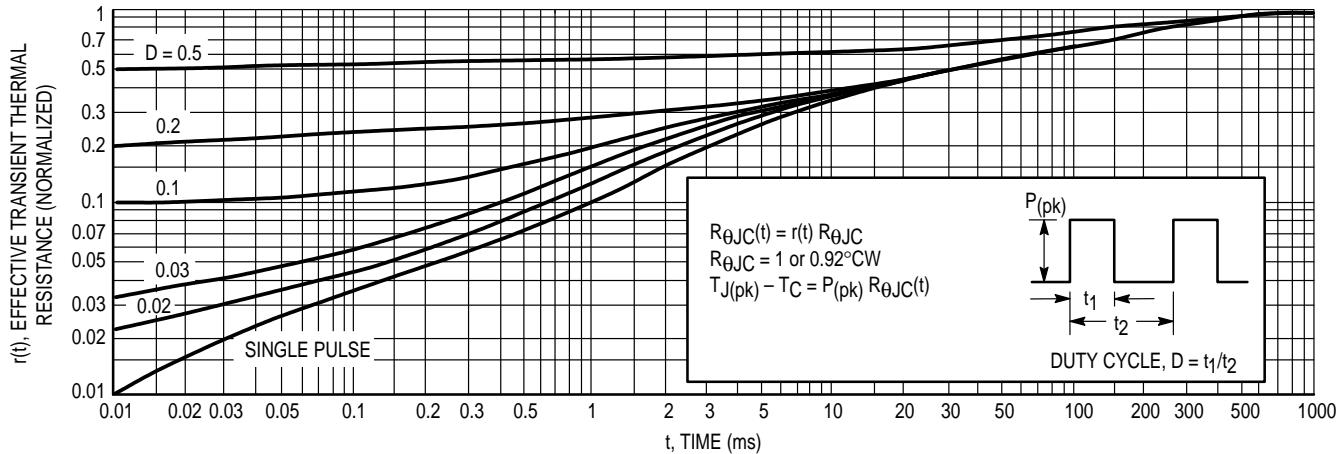


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_{\text{C}} - V_{\text{CE}}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_{\text{C}} = 25^{\circ}\text{C}$; $T_{\text{J(pk)}}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_{\text{C}} \geq 25^{\circ}\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{\text{J(pk)}}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter

voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{\text{CEO(sus)}}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{\text{CEO(sus)}}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

4. OPERATION ABOVE $V_{\text{CEO(sus)}}$ —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)**5. RBSOA —**

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

6. DESIGN SAMPLES —

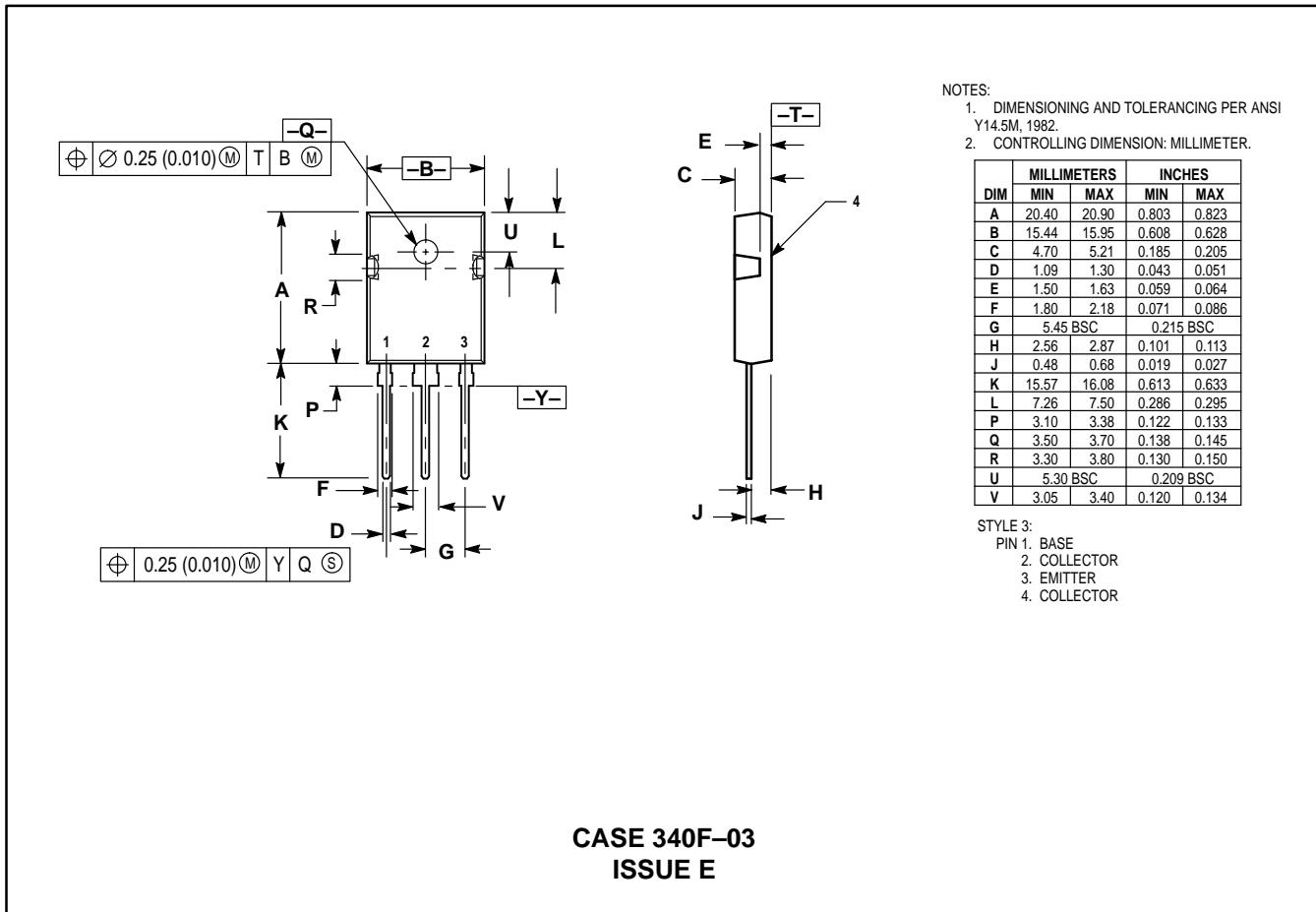
Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one de-

vice to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

PACKAGE DIMENSIONS



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How to reach us:

USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com – **TOUCHTONE** (602) 244-6609
INTERNET: <http://Design-NET.com>

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

